Modular Multilevel Converter-Based Bipolar High-Voltage Pulse Generator With Sensorless Capacitor Voltage Balancing Technique

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***Abstract*— In order to generate bipolar high-voltage (HV) pulses across certain load from HV dc (HVdc) power supply, a voltage source inverter (VSI) stage should be inserted between the load and the supply. In order to meet the required HV level, series connection of semiconductor devices should be employed with dynamic voltage sharing between the involved devices. Modular multilevel converter (MMC) can be used instead of the conventional two-level VSI to alleviate the complexity introduced by the deployment of series-connected devices. The voltage level of the HVdc power supply and the voltage rating of the available semiconductor devices determine the suitable number of MMC voltage levels (*N*). Capacitor voltage balancing is a vital issue for proper operation of the MMC. In general, conventional sensor-based balancing techniques require a significant amount of measurements, which increases the complexity of the system. In addition, the high dv/dt during switching times causes electromagnetic interference, which may adversely affect the accuracy of the measurements. In this paper, a sensorless voltage balancing technique is proposed for the MMC-based bipolar HV pulse generator that reduces the system sensitivity, cost, and complexity. A detailed illustration of the proposed approach is presented in this paper. The simulation and experimental results are used to validate the proposed concept.**

***Index Terms*— Bipolar pulse generation, modular multilevel converter (MMC), sensorless voltage balancing.**

I. Introduction

BIPOLAR high-voltage (HV) pulse generators are commonly used in different applications [1]–[3]. There are different methods to generate bipolar HV pulses in [1]–[11]. Employment of HV dc (HVdc) power supply with a voltage source inverter (VSI) is the most common method.

Nevertheless, in order to meet the HV level requirements, the HV switches are implemented via series-connected semiconductor devices as shown in Fig. 1. To ensure successful operation of the series-connected devices, dynamic voltage sharing should be considered through actively controlling the gate [12], which increases the complexity of the system. Alternatively, multistage cascaded H-bridge multilevel inverter with isolated voltage sources can be used as in [1]. In this method, the multistacked H-bridge stages are linked up in series to feed the pulsed load. The main disadvantage of the multistage cascaded H-bridge-based pulse generator is the need for isolated voltage sources.

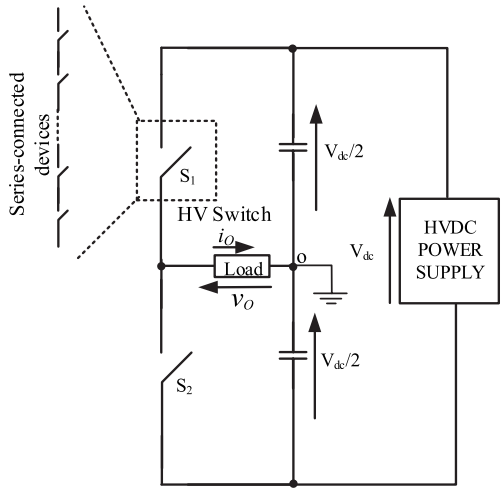

Fig. 1. Conventional bipole HV pulse generator.

Marx generator with an HV H-bridge at the load side can also be used effectively [2], [5], but the HV switches in the H-bridge should be implemented by series-connected devices with static and dynamic voltage sharing, which increases the complexity of the system.

In [6] and [7], a push-pull inverter-based HV bipolar pulse generator is proposed, but an HV switch is needed at the output stage (i.e., stacked devices should be employed).

In [13], a new technique for uniform voltage sharing in series-stacked semiconductor devices is proposed.

In [8], [10], and [11], new solid-state Marx topologies have been proposed for unipolar and bipolar pulse generation, but relatively a high number of semiconductor switches are required.

In [9], a new modular solid-state switch is proposed as a replacement to the HV switch (i.e., replacement for the series-connected devices).

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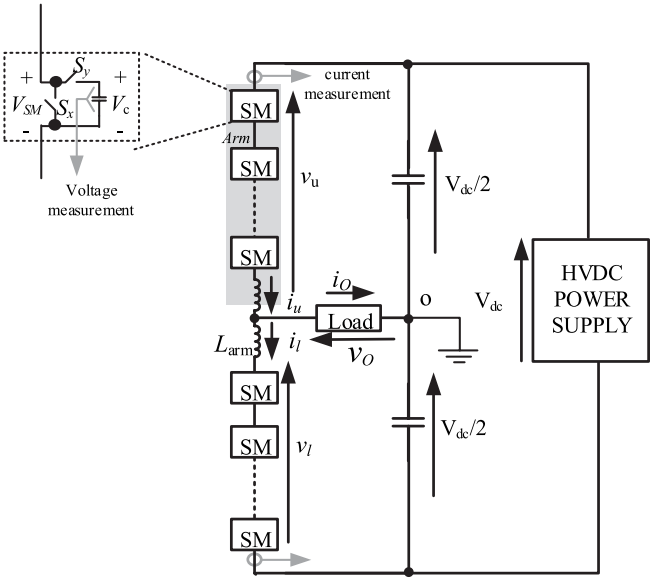

Fig. 2. MMC with sensor-based capacitor voltage balancing.

In [14] and [15], modular switched capacitor pulsed power generators as new arrangements for the capacitor-diode voltage multipliers are presented to keep the voltage rating and the number of components as minimum as possible for HV applications. This type of HV pulse generator generates unipolar output pulses. To obtain bipolar output pulses, an HV H-bridge at the load side should be employed.

Recently, modular multilevel converter (MMC) can be considered as one of the most promising VSIs in HV applications due to its modularity and scalability [16]. MMC-based systems provide employment of relatively low voltage semiconductor devices to generate HV output pulse without series-connected devices.

In this paper, an HVdc power supply in conjunction with MMC is used to generate bipole HV pulses. The basic concept of MMC is the cascaded connection of cells or submodules (SMs) per arm, as shown in Fig. 2. Based on the total HVdc input and the voltage rating of the available semiconductor devices, the number of SMs per arm can be determined. Capacitor voltage balancing in MMC is an essential process to ensure successful operation. Conventionally, based on the instantaneous value of the desired arm voltage (v_u for the upper arm), a certain number of SMs should be included in the arm current path and others should be bypassed. The decision of which SMs should be included is made based on the direction of the arm current to ensure operation with successful voltage balancing, i.e., to keep capacitors' voltages within desired window [17]. When MMC is used with sensor-based balancing technique in HV pulsed applications, the generated electromagnetic interference (EMI) due to high *dv*/*dt* during switching times may affect the accuracy of the measured signals [18].

In [9] and [19], stacked cells in MMC-based HV pulse generator have been used with additional diodes to balance the capacitor voltages, i.e., additional hardware components are used to ensure voltage balancing, which increases the system cost.

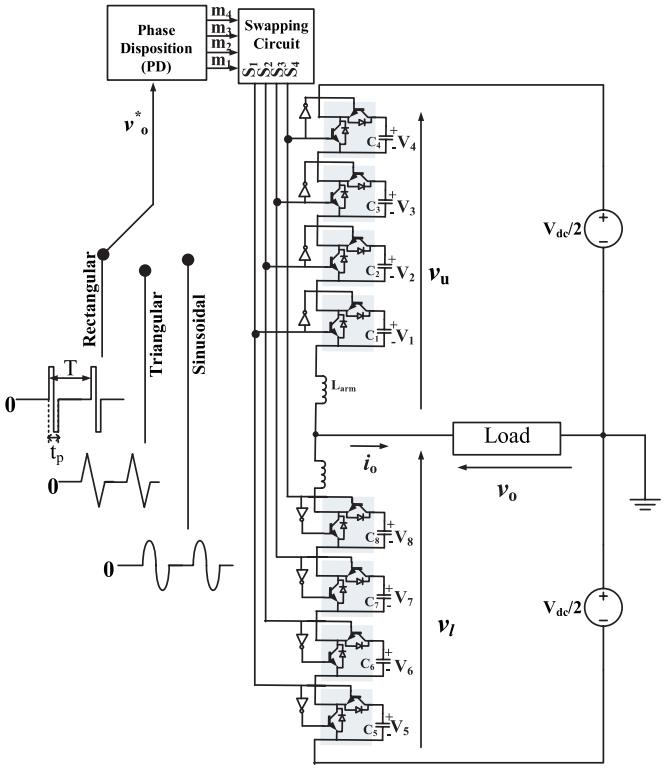

Fig. 3. Five-level MMC-based bipole HV pulse generator with the proposed sensorless voltage balancing technique.

In this paper, a sensorless capacitor voltage balancing technique is proposed to reduce the effect of EMI on the performance of the system and avoid employment of extra hardware components for voltage balancing (i.e., applying MMC-based HV pulse generator concept with a reduced cost and increased reliability).

The main advantages of the proposed approach can be summarized as follows:

1) operation with a sensorless voltage balancing technique for MMC-based bipole HV pulse generator, which reduces the system sensitivity, cost, and complexity;
2) employment of relatively low voltage devices to generate HV output pulses;
3) ability to generate different shapes of output pulses such as rectangular, triangular, and sinusoidal (i.e., flexible pulse pattern);
4) ability to control the output voltage magnitude.

A detailed analysis of the proposed sensorless voltage balancing algorithm is presented in this paper. A simulation model for a five-level MMC is used to validate the proposed approach, assuming different types of pulse patterns. Finally, a scaled down prototype for a three-level MMC is used to validate the proposed concept. The simulation and experimental results elucidate the effectiveness of the proposed sensorless voltage balancing approach in HV pulsed applications.

II. MMC Basics

The basic configuration and principle of operation of a conventional MMC system are shown in Fig. 2. The leg of MMC consists of two arms (upper and lower arms). Each arm

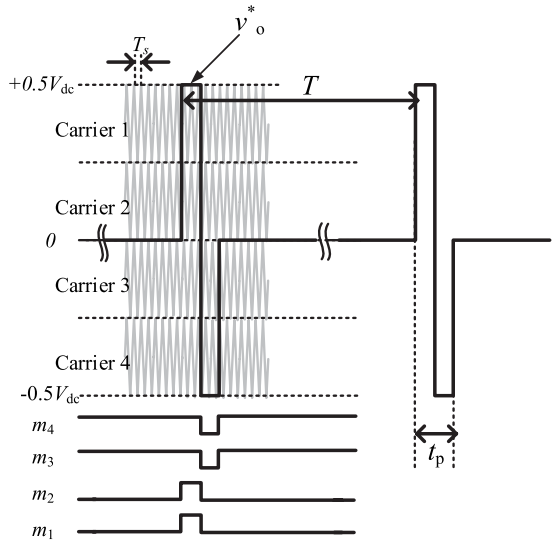

Fig. 4. PD pulses generation for an output voltage magnitude of $V_{dc}/2$.

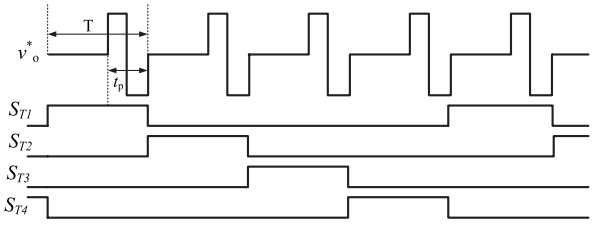

Fig. 5. Generation of balancing signals.

consists of $(N-1)$ half-bridge SMs, where N is the number of the converter phase voltage levels. The SMs' capacitances should be carefully selected to obtain acceptable capacitor voltage ripples at the highest loading condition.

The voltage of each SM capacitor is $[V_c = V_{dc}/(N-1)]$. The SM voltage (V_{SM}) can be zero (when S_x is turned ON and S_y is turned OFF), or V_c (when S_x is turned OFF and S_y is turned ON). Based on Fig. 2, the arm reference voltages are given by

$$v_u^* = \frac{V_{dc}}{2} - v_o^*, v_l^* = \frac{V_{dc}}{2} + v_o^* \quad (1)$$

where v_u^* and v_l^* are the upper and lower voltage references, respectively, while v_o^* is the desired output voltage where its magnitude can be controlled from zero up to $(V_{dc}/2)$.

In the sensor-based capacitor voltage balancing technique, all capacitors' voltages and arm currents should be measured to ensure successful operation of the MMC. With respect to the upper arm, based on the instantaneous value of the upper arm voltage reference (v_u^*) and the upper arm current direction (i_u), a certain number of SMs (k) will be activated where $0 \leq k \leq (N-1)$.

In case of a positive arm current, cells with lowest voltages are selected and vice versa. On the other hand, the number of cells to be active in the lower arm can be estimated by subtracting the extracted number of activated cells in the upper arm from $(N-1)$, and therefore the total number of activated cells equals $(N-1)$ in the converter leg, i.e., the corresponding total number of cells to be activated in the lower arm will be $(N-1-k)$. Based on the lower arm current direction (i_l), proper $(N-1-k)$ cells in the lower arm can be selected. Among the different modulation techniques, phase disposition (PD) modulation technique [17] is commonly used

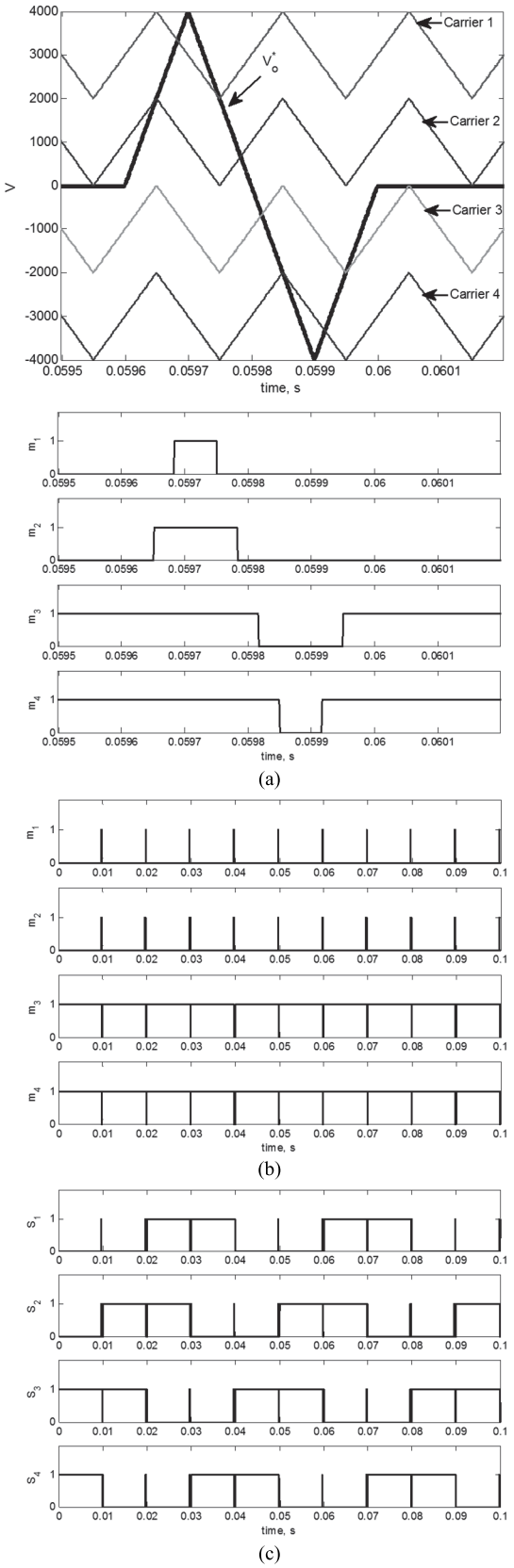

Fig. 6. Pulses generation. (a) PD. (b) PD pulses. (c) Gating pulses.

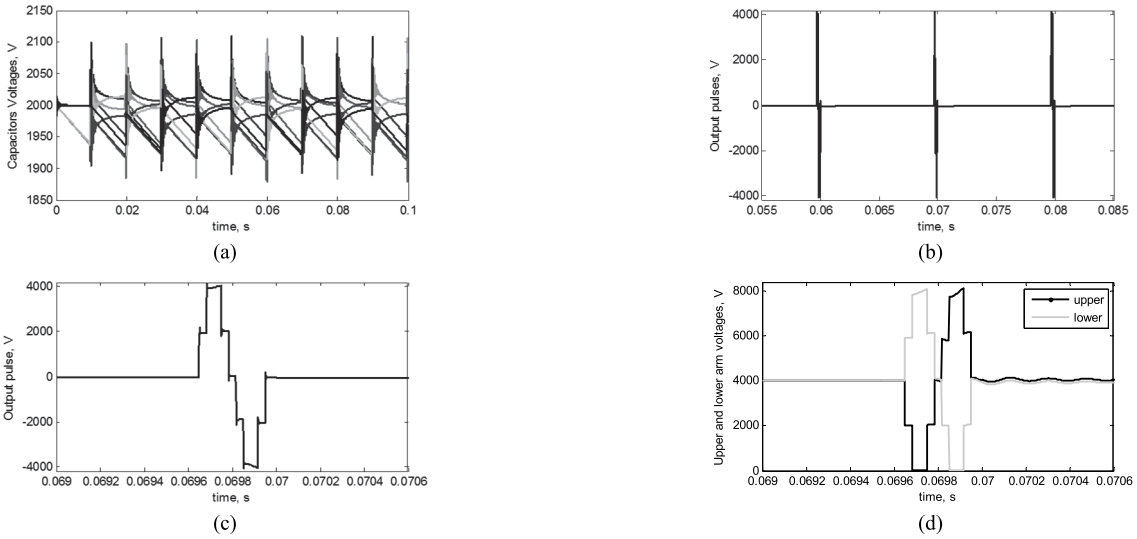

Fig. 7. Simulation results for triangular HV pulse generation. (a) Capacitors' voltages. (b) Output voltage. (c) Output bipolar pulse. (d) Upper and lower arm voltages.

to determine the required number of SMs to be activated in the upper arm. The number of required SMs to be activated is continuously changing with the variation of the arm voltage reference.

In this paper, a sensorless capacitor voltage balancing technique is proposed to reduce the system complexity and cost. In addition to these features, working without sensors in pulsed power applications is recommended to avoid the possible effect of the generated EMI on the accuracy of the measured signals due to the high *dv*/*dt* during switching times [18], [20]–[22]. The principle of operation of the proposed sensorless balancing technique is described in the following section.

III. Proposed Sensorless Capacitor Voltage Balancing for MMC-Based HV Pulse Generator

In this paper, a sensorless voltage balancing technique for an N-level MMC-based bipole HV pulse generator is proposed. In this technique, the pulses generated by the PD modulation technique are exchanged each fundamental cycle of the output voltage (T) among the SMs to guarantee the exposure of the SMs to the same loading conditions resulting in balanced capacitors' voltages.

A. Principle of Operation

The illustration of the proposed technique is based on a five-level MMC as shown in Fig. 3. In the proposed scheme, the gate pulses should be arranged as shown in Fig. 3 to guarantee that the total number of activated cells per leg is $(N-1)$, where N is the number of converter voltage levels.

The five-level MMC-based bipole HV pulse generator consists of two arms (upper and lower arms). Each arm consists of four SMs and one inductor (L_{arm}). It has to be noted that, before starting the MMC operation, each SM's capacitor should be precharged to a certain voltage level, which equals $V_{\text{dc}}/(N-1)$ to avoid starting transients, i.e., relatively low voltage external dc supply (external charger) can be used to achieve this task.

TABLE I
Swapping the PD Pulses Every Fundamental Cycle

Gate pulses	1st T	2nd T	3rd T	4th T	5th T
S_1	m_1	m_2	m_3	m_4	m_1 ….
S_2	m_2	m_3	m_4	m_1	m_2 ….
S_3	m_3	m_4	m_1	m_2	m_3 ….
S_4	m_4	m_1	m_2	m_3	m_4 ….

TABLE II
Simulation Parameters

Parameter	**Value**
Converter power rating	650W
Total input DC voltage , V_{dc}	8kV
Load resistance	1kΩ
Arm inductor	0.5mH, 2Ω internal resistance
SM capacitance	3μF, pre-charged voltage=2kV
Pulse specifications	T=0.01s, t_{p}=400μs, $\pm V_{\text{dc}}/2$
Carrier frequency	5kHz (=2× $\frac{1}{t_p}$)

In the proposed scheme, the PD modulation scheme is first used to generate pulses m_1–m_4 by comparing the output voltage reference with carriers 1-4, respectively, as shown in Fig. 4 (assuming rectangular output voltage).

It has to be noted that, in the case of triangular and sinusoidal pulse shapes, to obtain an accepted stepped output voltage, the frequency of the carrier signals ($f_s = 1/T_s$) should be multiple of $1/t_p$, where t_p is the bipole pulsewidth as shown in Fig. 4. Finally, the generated pulses (m_1–m_4) are exchanged each fundamental cycle (T) between SMs, i.e., the gate switching pulses for SMs (S_1–S_4) are shown in Table I. These pulses (S_1–S_4) and their complement are used to operate the SMs in upper and lower arms.

It is clear from Table I that the switching pattern will achieve a complete rotation every four fundamental cycles. In general, for an N-level inverter, the switching pattern will achieve a complete rotation every $(N-1)$ fundamental cycles.

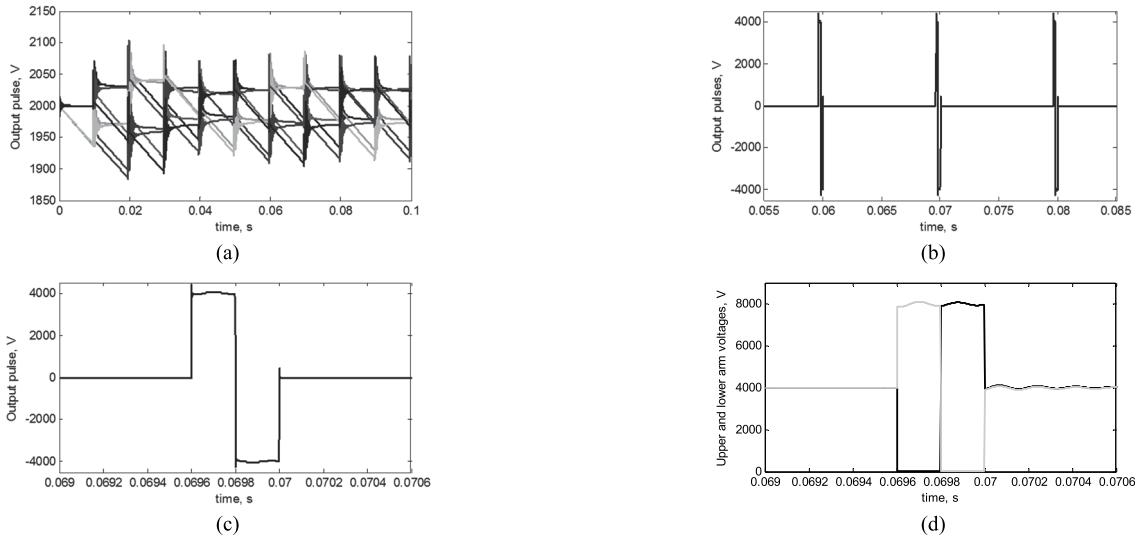

Fig. 8. Simulation results for rectangular HV pulse generation. (a) Capacitors' voltages. (b) Output voltage. (c) Output bipolar pulse. (d) Upper and lower arm voltages.

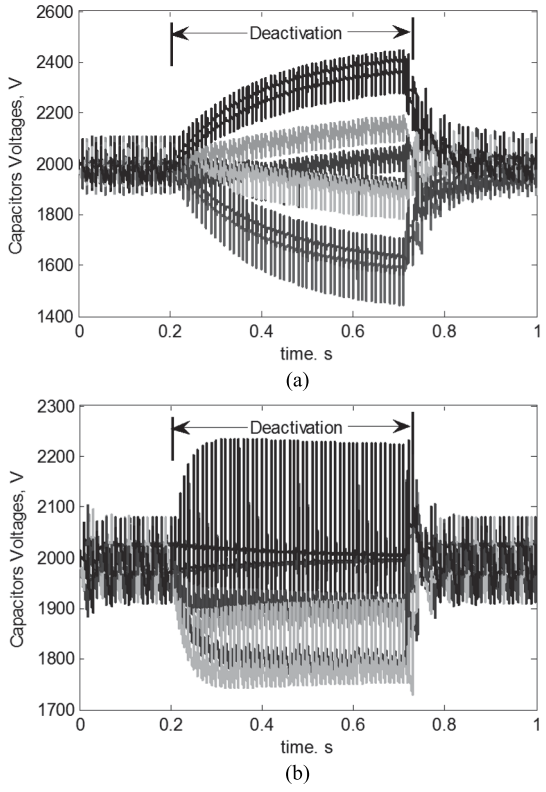

Fig. 9. Effect of the deactivation of the proposed sensorless balancing technique on the capacitors' voltages (a) triangular and (b) rectangular bipolar pulse generation.

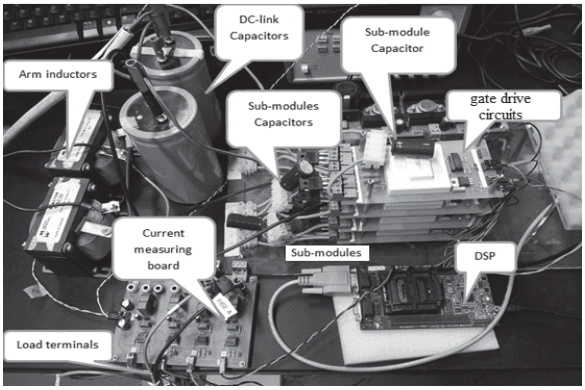

Fig. 10. Experimental prototype.

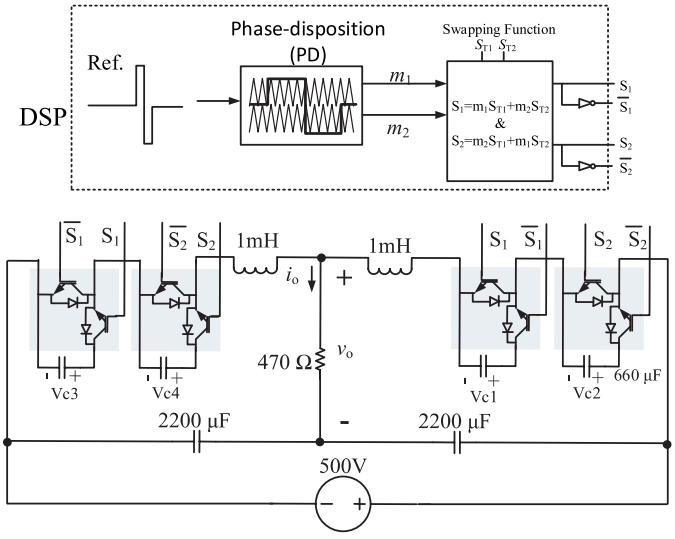

Fig. 11. Equivalent electrical power and control circuits of the experimental setup.

B. Swapping Circuit

A swapping circuit, shown in Fig. 3, is used to obtain the desired switching pattern illustrated in Table I. It should be noted that the function of this circuit will be programmed on the controller chip (software based), i.e., no need for any additional hardware circuits. To achieve the needed functionality, a set of signals should be generated internally inside the controller, which generally consists of $(N-1)$ pulsed signals $[S_{T1}–S_{T(N-1)}]$. These pulsed signals are synchronized with the reference signal (v_o^*) as shown in Fig. 5. The pulsewidth and period of each pulsed signal

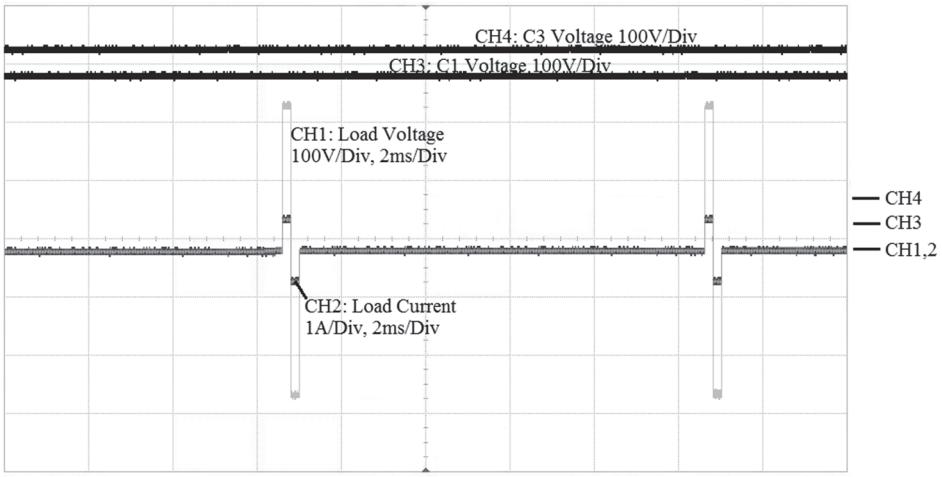

Fig. 12. Experimental results.

TABLE III
EXPERIMENTAL SETUP PARAMETERS

Parameter	Value
V_{dc}	500V
SM capacitance	660μF
DC-link capacitance	2200 μF
Arm inductor	1mH
Carrier frequency	1kHz
Load resistance	470Ω
Pulse specifications	Rectangular ±250V, T=0.01s, t_p=400μs

are T and $(N-1)T$, respectively, and the time shift between rising edges of any two successive pulsed signals is T as shown in Fig. 5.

The aforementioned set of signals (S_{T1}–S_{T4}) and PD output pulses (m_1–m_4) are fed into a simple digital logic circuit (swapping circuit) to generate the desired switching pattern (S_1–S_4). The gate pulses (S_1–S_4) can be expressed by

$$\begin{aligned} S_1 &= m_1 S_{T1} + m_2 S_{T2} + m_3 S_{T3} + m_4 S_{T4} \\ S_2 &= m_2 S_{T1} + m_3 S_{T2} + m_4 S_{T3} + m_1 S_{T4} \\ S_3 &= m_3 S_{T1} + m_4 S_{T2} + m_1 S_{T3} + m_2 S_{T4} \\ S_4 &= m_4 S_{T1} + m_1 S_{T2} + m_2 S_{T3} + m_3 S_{T4}. \end{aligned} \tag{2}$$

Applying the swapping technique, the generated gate pulses (S_1–S_4) are identical, but shifted in time. This guarantees balancing of capacitors' voltages, which means that the average charge of each capacitor will be equal, i.e., capacitors' voltages can be kept within a certain voltage window.

IV. SIMULATION

A simulation model for a five-level MMC-based bipolar HV pulse generator has been built with the parameters given in Table II.

A. Dynamic Performance

Different pulse shapes are tested (triangular and rectangular) with the specifications given in Table II. The PD pulses (m_1–m_4) can be generated by comparing the output voltage reference (v_o^*) with the carrier signals as shown in Fig. 6(a). It is clear that the generated PD pulses have different pulsewidths as shown in Fig. 6(a) and (b). By swapping these pulses among SMs as in (2), the corresponding gating pulses (S_1–S_4) are as shown in Fig. 6(c). It is clear that the gating signals (S_1–S_4) are identical, but shifted in time, which means that the average charge of each capacitor will be equal, i.e., capacitor voltages can be kept balanced.

The corresponding simulation results for triangular and rectangular pulses are shown in Figs. 7 and 8, respectively. Figs. 7(a) and 8(a) show that the proposed sensorless capacitor voltage balancing is able to keep the capacitors' voltages within a certain voltage window. Figs. 7(b) and 8(b) show the output train of pulses for triangular and rectangular bipolar pulse generation, respectively. The zoomed-in versions of the output pulsed voltage in both cases are shown in Figs. 7(c) and 8(c), while the corresponding upper and lower arm voltages in both cases are shown in Figs. 7(d) and 8(d). It is clear that the upper and lower arm voltages are unipolar voltages ranging from zero to V_{dc}.

B. Effect of Deactivation of the Proposed Balancing Technique

To show the effectiveness of the proposed sensorless capacitor voltage balancing technique, the technique is deactivated at $t = 0.2$ s by directly connecting the PD signals (m_1–m_4) to gate pulses (S_1–S_4) without swapping.

Then it is activated again at $t = 0.7$ s by applying the swapping concept again as in (2). The corresponding capacitors' voltage variations for triangular and rectangular bipolar pulse generation are shown in Fig. 9(a) and (b), respectively. It is clear that when the balancing technique is deactivated, some of the SMs suffer from a voltage increase due to unequal loading of the capacitors. This voltage increase may damage the involved SMs components if it becomes higher than the safe operating voltage. It is also clear that when the balancing technique is activated again, the capacitors' voltages converge and return back successfully to their normal voltage window.

V. EXPERIMENTAL RESULTS

To validate the proposed sensorless capacitor voltage balancing technique in MMC-based bipole HV pulse generator,

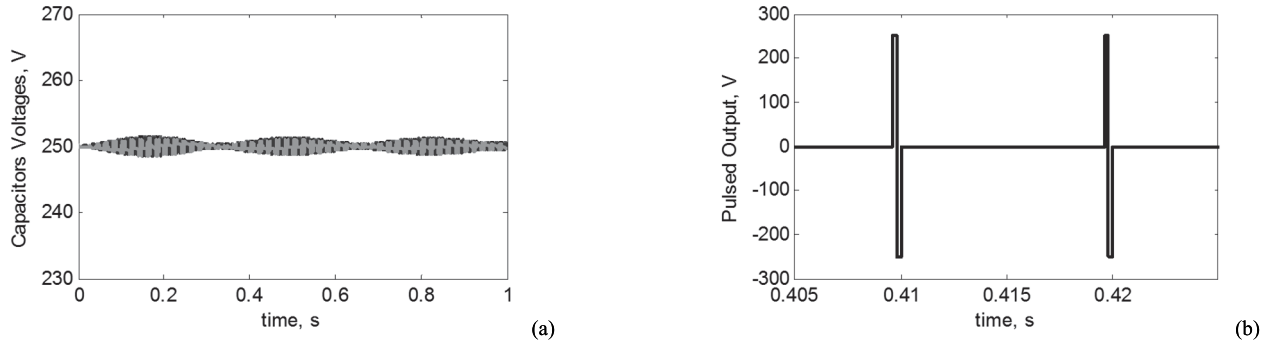

Fig. 13. Simulation results for the experimental setup. (a) Capacitors voltages, (b) Pulsed output.

a scaled experimental prototype of three-level MMC feeding a resistive load has been implemented as shown in Fig. 10. The experimental setup parameters are given in Table III. The equivalent electrical power and control circuits of the experimental setup are shown in Fig. 11. A TI-TMS320F2812 Digital Signal Processor program has been developed to execute the function of the swapping circuit described in Fig. 11. The corresponding experimental results are shown in Fig. 12 where the capacitors' voltages are balanced and the bipolar train of pulses is generated successfully. The simulation results for the experimental setup are shown in Fig. 13. It is clear that the simulation and experimental results are very close.

VI. Conclusion

In this paper, an MMC-based bipolar HV pulse generator with sensorless voltage balancing technique is proposed. The proposed balancing technique adds no cost to the system and reduces the effect of generated EMI, due to high *dv*/*dt*, on the system performance as there are no voltage/current measurement boards in the proposed scheme for capacitor voltage balancing. The proposed approach also provides employment of relatively low voltage devices to generate HV output pulses. It has also a flexible pulse output pattern as well as its ability to control the output voltage magnitude. A detailed analysis of the proposed sensorless voltage balancing algorithm is presented. The simulation and experimental results show the effectiveness of the proposed sensorless voltage balancing approach in the HV pulsed applications. The limitations of the proposed approach are the number of employed SMs and the frequency of pulsed output. As the number of employed SMs increases or frequency of pulsed output decreases, the voltage ripples of SMs' capacitors increase. Therefore, proper selection of capacitance value, based on these factors in addition to the power level of the load, is an essential design aspect.

Acknowledgment

The statements made herein are solely the responsibility of the authors.

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